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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. DP-652 US
Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

AN INPUT/OUTPUT PROTECTION DEVICE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT

and invented by:

Yasuyuki Morishita

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **18** pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☐ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets **5 (Figs. 1A-5B)**
   b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
    ☐ First Class ☐ Express Mail *(Specify Label No.):* _____

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Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	20	- 20 =	0	x	$18.00	$0.00
Indep. Claims	1	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE *(specify purpose)*		**Assignment Recordation**				$40.00
					TOTAL FILING FEE	$730.00

☒ A check in the amount of **$730.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **50-0481** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: **July 19, 2000**

Sean M. McGinn, Esq.
Reg. No.: 34,386

cc:

Customer No.: 21254

DP-652 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Morishita, Y.

Serial No.: Not Yet Assigned — Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith — Examiner: Unknown

For: AN INPUT/OUTPUT PROTECTION DEVICE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits and calculation of the filing fee, please amend the above-identified application as follows:

IN THE CLAIMS:

Claim 4, line 2, delete "or 3".

Claim 5, lines 1-2, delete "one of claims 1 to 4" and insert --claim 1--.

Claim 6, lines 1-2, delete "one of claims 1 to 5" and insert --claim 1--.

Claim 7, lines 1-2, delete "one of claims 1 to 5" and insert --claim 1--.

Claim 8, lines 1-2, delete "one of claim 6 or 7" and insert --claim 6--.

Claim 9, lines 1-2, delete "one of claim 7 or 8" and insert --claim 7--.

Claim 10, line 2, delete "one of claim 7 or 8" and insert --claim 7--.

Claim 11, lines 1-2, delete "one of claims 1 to 10" and insert --claim 1--.

Claim 12. Lines 1-2, delete "one of claims 1 to 10" and insert --claim 1--.

Please add the following new claims:

--13. An input/output protection device in accordance with claim 3, wherein the third diffusion layer has a depth equal to or more than that of the fourth diffusion layer.

14. An input/output protection device in accordance with claim 2, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

15. An input/output protection device in accordance with claim 3, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

16. An input/output protection device in accordance with claim 4, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

17. An input/output protection device in accordance with claim 2, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

18. An input/output protection device in accordance with claim 3, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

19. An input/output protection device in accordance with claim 4, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

20. An input/output protection device in accordance with claim 5, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.--

REMARKS

The above changes to the claims have been made, and new claims have been added, to delete the multiple-dependency of the claims.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

Sean M. McGinn
Registration No.: 34,386

Date: 7/19/05

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

Title: AN INPUT/OUTPUT PROTECTION DEVICE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT

INVENTOR(S): YASUYUKI MORISHITA

AN INPUT/OUTPUT PROTECTION DEVICE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to an input/output protection device for a semiconductor integrated circuit.

Description of the Prior Art

In general, since complementary metal oxide semiconductor (CMOS) transistors included in a semiconductor integrated circuit become quite smaller in size, it is increasingly difficult for an input/output protection device for such a semiconductor integrated circuit to protect the device against electrostatic discharge (ESD). That is, when the CMOS transistor including a gate oxide film is reduced in size, the film becomes thinner and hence its dielectric tolerance is decreased. Recently, to reduce parasitic resistance of such a transistor including a diffusion layer, a metal silicidation of the diffusion layer has been applied. This also causes lowering ESD tolerance.

Heretofore, a parasitic lateral type bipolar transistor has been employed as a semiconductor integrated circuit including a CMOS of the prior art. Various techniques of this kind have been proposed in various articles, for example, in the Japanese Patent Laid-Open Nos. 8-51188 and 7-122715.

Referring now to Figs. 5A and 5B, description will be given of a representative example of an input/output protection device including a bipolar transistor of parasitic lateral type of the prior art. Fig. 5A shows in a plan view the input/output protection device. Fig. 5B is a cross-sectional view thereof along a direction X-Y of Fig. 5A. As can be seen from Fig. 5B, this configuration includes a p-type well layer 102 on a surface of a p-type silicon substrate 101. On a surface of p-type well layer 102, a device isolation film 103 is selectively fabricated.

Moreover, an n-type first diffusion layer 104 is formed on a surface of p-type well layer 102 and an n-type second diffusion layer 105 is manufactured on another surface of p-type well layer 102. The configuration further includes a p-type lead diffusion layer 106. First and second diffusion layers 104 and 105 are manufactured in a process in which a diffusion layer is formed as a source-drain region of a CMOS transistor.

In this structure, first diffusion layer 104 is connected to an input/output terminal 107. Second diffusion layer 105 and diffusion layer 106 are linked with a ground terminal 108.

In the input/output protection device configured as above, when a positive, high-voltage pulse is applied to input/output terminal 107, an avalanche breakdown takes place in a region of junction between first diffusion layer 104 and p-type well layer 102. This causes a breakdown current to flow from input/output terminal 107 to diffusion layer 106. The breakdown current locally increases potential in p-type well layer 102 to operate a bipolar transistor of lateral type including first diffusion layer 104 as a collector, second diffusion layer 105 as an emitter, and p-type well layer 102 as a base. As a result of operation of this transistor, i.e., a parasitic bipolar transistor, ESD current flows from input/output terminal 107 via second diffusion layer 105 as the emitter to ground terminal 108.

Since the degree of integration of semiconductor integrated circuits is increased and its operation speed becomes higher, semiconductor elements of these circuits are decreased in size and the density thereof becomes greater. In general, this resultantly increases the number of defects in the semiconductor elements due to electrostatic discharge (ESD).

The bipolar transistor of parasitic lateral type cannot appropriately respond to a positive high-voltage pulse with a high-

speed or a steep rising edge. Consequently, before the protection device starts its functions, a gate oxide film in its internal circuit is possibly destroyed in many cases. As the size of semiconductor integrated circuits is decreased, the gate oxide film becomes thinner and therefore is more easily destroyed.

In the bipolar input/output protection device of lateral type above, the breakdown current after the avalanche breakdown flows through a region of p-type well layer 102 having lower resistance than p-type silicon substrate 101. Therefore, potential of p-type well layer 102 as the base of the bipolar transistor cannot be quickly increased. This leads to a problem of a slow response of the input/output protection device. The goal of the present invention provides to a lateral bipolar type input/output protection device which rapidly responds to an over voltage pulse and / or over current.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an input/output protection device of a lateral bipolar type having a high response to an excess voltage pulse and/or an excess current pulse associated with, for example, ESD phenomena.

In accordance with the present invention, there is provided an input/output protection device for a semiconductor integrated circuit including a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring. The device includes a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the layer having a second conduction type opposite to the first conduction type and being connected to the input/output terminal; a second diffusion layer of the second conduction type connected to the electrode wiring kept, the electrode wiring being at a predetermined potential; and a third

diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer. The first diffusion layer is circularly enclosed with the second and third diffusion layers.

In the configuration, the region of the first conduction type of the semiconductor substrate includes a fourth diffusion layer having an impurity concentration higher than that of the semiconductor substrate. The impurity concentration of the fourth diffusion layer monotonously decreases in a direction from a surface of the semiconductor substrate to an inner section thereof. The third diffusion layer has a depth equal to or more than that of the fourth diffusion layer.

When a high voltage is applied to the input/output terminal, there is formed and is operated a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base.

In the input/output protection device for a semiconductor integrated circuit in accordance with the present invention, the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate. Alternatively, the first and second diffusion layers are fabricated with a gate electrode disposed on a surface of the semiconductor substrate. In the structure, the device separating isolation layer or the gate electrode is fabricated in a circular contour.

Additionally, the gate electrode is connected to the signal wiring of the internal circuit of the semiconductor integrated circuit. The gate electrode is fixed to a predetermined potential.

In the input/output protection device for a semiconductor integrated circuit above, the first conduction type is a p type and the second conduction type is an n type, or the first conduction type is an n

type and the second conduction type is a p type. The predetermined potential is a potential of a power source.

As above, In the input/output protection device for a semiconductor integrated circuit in accordance with the present invention, the first diffusion layer as the collector region of the parasitic, lateral bipolar transistor is circularly enclosed with the third diffusion layer. Consequently, the breakdown current appearing at occurrence of an avalanche breakdown in a junction region between the first diffusion and the region of the first conduction type flows laterally in the third diffusion layer. This current is however hindered therein and flows in a deep inner region of the semiconductor substrate. In a usual semiconductor substrate which has a low impurity concentration and hence high resistance, when the breakdown current flows in an inner region of the substrate, there occurs a voltage drop by the current. As a result, the potential of the base region, i.e., the fourth diffusion layer of the region or the first conduction type can be easily increased. This facilitates operation of the bipolar transistor. Consequently, the input/output protection device can quickly responds to the excess voltage pulse or the excess current pulse of, for example, ESD phenomena. The device can therefore satisfactorily achieve the protecting operation even when the semiconductor integrated circuit becomes finer in size.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and features of the present invention will become more apparent from the consideration of the following detailed description taken in conjunction with the accompanying drawings in which:

Figs. 1A and 1B are a plane view and a cross-sectional view for explaining a first embodiment of an input/output protection device

for a semiconductor integrated circuit in accordance with the present invention;

Fig. 2 is a graph showing a distribution of impurity concentration for explaining the first embodiment of the present invention;

Figs. 3A and 3B are a plane view and a cross-sectional view for explaining a second embodiment of an input/output protection device for a semiconductor integrated circuit in accordance with the present invention;

Fig. 4 is a plane view of an input/output protection device for explaining a third embodiment in accordance with the present invention; and

Figs. 5A and 5B are a plane view and a cross-sectional view for explaining a first embodiment of an input/output protection device in the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring next to Figs. 1A, 1B, and 2, description will be given of a first embodiment in accordance with the present invention. Fig. 1A shows in a plane view an input/output protection device for a semiconductor integrated circuit in accordance with the present invention. Fig. 1B shows in a cross-sectional view a configuration of the input/output device shown in Fig. 1A. Fig. 2 is a graph to explain a distribution of impurity concentration in a region serving as a base of a parasitic, bipolar transistor.

As shown in Fig. 1B, on a surface of a p-type silicon substrate having an impurity concentration of about 10^{15} atoms/cm^3, a fourth diffusion layer 2, 2a is fabricated in a similar fashion as described in conjunction with the prior art above. The layer 2, 2a has an impurity concentration of about 10^{17} atoms/cm^3 and a depth of about one

micrometer (μ m). On a surface of fourth diffusion layer 2, 2a, a device separating isolation layer 3 is selectively formed as can be seen from Figs. 1A and 1B. The isolation layer 3 is fabricated by known local oxidation of silicon (LOCOS) or by trench isolation.

Manufactured on a surface of fourth diffusion layer 2, 2a are an n-type first diffusion layer 4 and an n-type second diffusion layer 5. Second diffusion layer 5 is formed to enclose or to surround first diffusion layer 4 as shown in Fig. 1A. There is also fabricated a p-type lead diffusion layer 6. First diffusion layer 4 or second diffusion layer 5 is formed in a process in which a diffusion layer is manufactured as a source-drain region of a CMOS transistor. Namely, the layer has an impurity concentration of about 10^{20} atoms/cm^3 and a depth of about 0.1 μ m. Depending on cases, a silicide layer may be fabricated on a surface of these diffusion layers.

In accordance with the present invention, as can be seen from Figs. 1A and 1B, a third diffusion layer 7 as electro-conductivity type is formed in a region associated with second diffusion layer 5. Layer 7 is be deeper than fourth diffusion layer 2, 2a. Layer 7 has a conduction type equal to that of second diffusion layer 5. Layer 7 is fabricated in a process in which an n-type well layer is formed in a semiconductor device manufacturing process. In Fig. 1A, region of third diffusion layer 7 is indicated by slant lines for easy explanation.

In this structure, first diffusion layer 4 is connected to an input/output terminal 8 in the same manner as for the prior art. Second diffusion layer 5 and diffusion layer 6 for drawing out or picking up are linked with a ground terminal 9.

In the input/output protection device configured as above, when a positive, high-voltage pulse is applied to input/output terminal 8, an avalanche breakdown occurs in a junction region between first and fourth diffusion layers 4 and 2a. In the constitution of the present

invention, a breakdown current caused by the avalanche breakdown flows in a longitudinal direction from first diffusion layer 4 via fourth diffusion layer 2a to silicon substrate 1. That is, as shown in Fig. 1B, fourth diffusion layer 2a is surrounded with third diffusion layer 7, and hence the breakdown current to laterally flow in fourth diffusion layer 2a is hindered.

As above, in accordance with the present invention, the breakdown current flows through silicon substrate 1 into diffusion layer 6. Resultantly, the breakdown current has an elongated path. In addition, silicon substrate 1 is lower in impurity concentration than fourth diffusion layer 2, 2a.

In consequence, in an initial stage of the avalanche breakdown, a voltage drop between a bottom surface of fourth diffusion layer 2a and diffusion layer 6 is increased. This makes it possible to increase the potential of fourth diffusion layer 2a at a higher speed.

Since the potential of fourth diffusion layer 2a is quickly increased by the breakdown current, a lateral, bipolar transistor including fourth diffusion layer 2a as a parasitic base region, first diffusion layer 4 as a collector, and second and third diffusion layers 5 and 7 as an emitter can operate at a higher speed as compared with the prior art.

By the operation of the transistor above, excess charge caused, for example, by ESD on input/output terminal 8 is discharged via second and third diffusion layers 5 and 7 service as the emitter of the transistor into ground terminal 9.

In accordance with the present invention, fourth diffusion layer 2a functioning as the parasitic base region of the transistor is enclosed with third diffusion layer 7. Therefore, the potential of fourth diffusion layer 2a is quickly increased and hence excess charge is discharged at a higher speed, i.e., parasitic bipolar transistor operate

quickly. As a result, the semiconductor integrated circuit is completely protected against ESD phenomena.

As shown in Fig. 1B, after the transistor starts its operation, the current flows via path I_1 to third diffusion layer 7 as the emitter region. This is because path I_2 is longer than path I_1. Consequently, parasitic bipolar action can easily occur on a surface area of fourth diffusion layer 2a. Description will next be given of a method of solving the problem above by referring to Fig. 2.

Fig. 2 shows in a graph a distribution of impurity concentration in a depth direction of a zone ranging from a junction plane between fourth and first diffusion layers 2a and 4 to silicon substrate 1. The impurity concentration of fourth diffusion layer 2a, 2 monotonously lowers in a direction toward silicon substrate 1 as shown in Fig. 2.

In the circuit including the configuration of fourth diffusion layer 2, 2a, when the lateral, bipolar transistor operates, the transistor shows an amplification factor (hFE) greater in path I_1 than in path I_2. Therefore, electrostatic discharge (ESD) takes place without any deviation with respect to the depth direction, namely, uniformly in the direction of depth of third diffusion layer 7. This consequently prevents destruction of the input/output protection device by strong heat produced when the electrostatic discharge locally occurs in a surface area of fourth diffusion layer 2a.

Referring now to Figs. 3A and 3B, description will be given of a second embodiment of the present invention. Fig. 3A shows in a plane view an input output protection device for a semiconductor integrated circuit in accordance with the present invention. Fig. 3B is a cross-sectional view of the embodiment taken along a line C-D of Fig. 3A. In Figs. 3A and 3B, the same constituent components as those shown in the first embodiment are assigned with the same reference numeral.

Like in the first embodiment, a fourth diffusion layer 2, 2a is manufactured on a surface of a p-type silicon substrate 1 as shown in Fig. 3B. On a surface of fourth diffusion layer 2, 2a, a device separating isolation layer 3 is selectively formed as can be seen from Figs. 3A and 3B.

On p-type well region 2, a gate electrode 10 having a closed ring shape is fabricated with a gate isolating film therebetween as shown in Figs. 3A and 3B. An n-type first diffusion layer 4 and an n-type second diffusion layer 5 are formed to match with a pattern of gate electrode 10. First diffusion layer 4 and/or second diffusion layer 5 is (are) employed as diffusion layers for a source-drain region of an MOS transistor.

The configuration further includes a p-type lead diffusion layer 6. As can be seen from Figs. 3A and 3B, a third diffusion layer 7a is fabricated in a partial region over second diffusion layer 5. Layer 7a is deeper than fourth diffusion layer 2, 2a. Third diffusion layer 7a is equal in conduction type to second diffusion layer 5. In Fig. 3A, an area of third diffusion layer 5 is hatched for easy understanding.

In this configuration, first diffusion layer is connected to an input/output terminal 8 in almost the same way as for the first embodiment. Second diffusion layer 5 and diffusion layer 6 are coupled with a ground terminal 9.

In the input/output protection device configured as above, when a positive, high-voltage pulse is applied to input/output terminal 8 as described in conjunction with the first embodiment, potential of fourth diffusion layer 2a to serve as a base region of a transistor is quickly increased by a breakdown current as above. This results in quick parasitic bipolar action of excess charge from input/output terminal 8. The semiconductor integrated circuit is therefore completely protected against ESD phenomena.

In the structure of the second embodiment, when input/output terminal 8 is used as an input terminal, gate electrode 10 is connected to a fixed terminal 11. Fixed terminal 11 is set to a ground potential. Conversely, when input/output terminal 8 is used as an output terminal, gate electrode 10 is connected to an internal circuit of the semiconductor integrated circuit.

Next, description will be given of a third embodiment of the present invention by referring to Fig. 4. Fig. 4 shows in a plane view an input/output protection device for a semiconductor integrated circuit in accordance with the present invention. The third embodiment differs in a pattern of the plane view from the first embodiment. These embodiments are in the cross-sectional configuration almost equal to the first embodiment. In Fig. 4, the same constituent components as those of the first embodiment are assigned with the same reference numerals.

Like in the first embodiment, a fourth diffusion layer 2a is formed on a surface of a p-type silicon substrate and a device separating isolation film 3, 3a is selectively manufactured on a surface of the fourth diffusion layer as shown in Fig. 4. On a p-type well region, device separating isolation film 3a is formed in a closed ring shape as can be seen from Fig. 4. There are fabricated an n-type first diffusion layer 4a and an n-type second diffusion layer 5a to match with a pattern of device separating isolation film 3a.

The configuration further includes a p-type lead diffusion layer 6. A third diffusion layer 7b is manufactured in an area over second diffusion layer 5a. Layer 7b is deeper than fourth diffusion layer. Third and second diffusion layers 7b and 5a are equal in the conduction type to each other. In Fig. 4, an area of third diffusion layer 7b is hatched for easy explanation.

In this structure, first diffusion layer 4a is connected to an

input/output terminal as shown in the configuration of the first embodiment. Second diffusion layer 5a and diffusion layer 6 are linked with a ground terminal.

The third embodiment leads to an advantage similar to that of the first embodiment. In this situation, first diffusion layer 4a has a circular periphery. Therefore, the avalanche breakdown described for the first embodiment uniformly takes place in the periphery of first diffusion layer 4a. This accordingly prevents the local electrostatic discharge in a surface area of the forth diffusion layer and hence completely protects the input/output protection device against destruction by strong heat.

In the description of the embodiments above, the input/output protection device is formed on a p-type silicon substrate. This however does not restrict the present invention. Namely, the present invention is also applicable to an n-type silicon substrate. However, in this case, the conduction type described above must be reversed. Moreover, ground terminal 9 and fixed terminal 11 must be replaced with a power source terminal. In this case, the semiconductor devices are effectively protected against a negative, high-voltage pulse. The present invention is also applicable even when the input/output protection device is fabricated in a p-type well or in an n-type well.

In the embodiments above, the fourth diffusion layer has a higher impurity concentration than the silicon substrate. However, the present invention can be similarly applied even when the fourth diffusion layer is absent in the configuration. In this case, the parasitic base region is a surface area of the silicon substrate.

In accordance with the present invention, first diffusion layer 4 may be enclosed in a ring shape with third diffusion layer 7 and a deep device separating isolation film. This device separating isolation film is different from device separating isolation film 3 and is almost

equal in depth to diffusion layer 7 prescribed the third embodiment.

Also in this situation, the breakdown current at occurrence of the avalanche breakdown in a junction region between the first diffusion layer and the region of the first conduction type laterally flows in deep third diffusion layer 7b and the deep device separating isolation film. However, the breakdown current is hindered and flows deep in an inner section of the semiconductor substrate. Consequently, as in the embodiments above, the absolute value of potential of the fourth diffusion layer of the region of the first conduction type as the base region can be easily increased. Namely, this easily causes the bipolar operation.

As above, in the input/output protection device for a semiconductor integrated circuit in accordance with the present invention, in a region of a first conduction type or a fourth diffusion layer of a semiconductor substrate, a first diffusion layer of a second conduction type opposite to the first conduction type is formed and is connected to an input output terminal and a second diffusion layer of the second conduction type is fabricated to be connected to electrode wiring at a fixed potential. At a bottom of the second diffusion layer, a third diffusion layer of the second conduction type is manufactured and is connected to the second diffusion layer. The first diffusion layer is circularly enclosed with the second and third diffusion layers.

When a high voltage is applied to the input/output terminal, a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is formed and is put to operation. The operation of the transistor causes ESD phenomena.

Thus, in order to the electrostatic discharge, the input/output protection device quickly responds to an excess voltage externally

applied to the input terminal. This increases the protective function of the protection device for the semiconductor integrated circuit.

To increase the degree of integration and/or the operation speed in a semiconductor integrated circuit, the constituent semiconductor devices become smaller in size and density thereof is increased in the semiconductor integrated circuit. Even in this situation, defects which may be caused in semiconductor devices by ESD phenomena or the like can be easily prevented in accordance with the present invention.

While the present invention has been described with reference to the particular illustrative embodiments, it is not to be restricted by those embodiments but only by the appended claims. It is to be appreciated that those skilled in the art can change or modify the embodiments without departing from the scope and spirit of the present invention.

WHAT IS CLAIMED IS:

1. An input/output protection device for a semiconductor integrated circuit including a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring, comprising:

a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the layer having a second conduction type opposite to the first conduction type and being connected to the input/output terminal;

a second diffusion layer of the second conduction type connected to the electrode wiring kept, the electrode wiring being at a predetermined potential; and

a third diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer,

the first diffusion layer being circularly enclosed with the third diffusion layers.

2. An input/output protection device in accordance with claim 1, wherein the region of the first conduction type of the semiconductor substrate includes a fourth diffusion layer having an impurity concentration higher than that of the semiconductor substrate.

3. An input/output protection device in accordance with claim 2, wherein the impurity concentration of the fourth diffusion layer monotonously decreases in a direction from a surface of the semiconductor substrate to an inner section thereof.

4. An input/output protection device in accordance with claim 2 or 3, wherein the third diffusion layer has a depth equal to or

more than that of the fourth diffusion layer.

5. An input/output protection device in accordance with one of claims 1 to 4, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

6. An input/output protection device in accordance with one of claims 1 to 5, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

7. An input/output protection device in accordance with one of claims 1 to 5, wherein the first and second diffusion layers are manufactured with a gate electrode disposed on a surface of the semiconductor substrate.

8. An input/output protection device in accordance with one of claim 6 or 7, wherein the device separating isolation layer or the gate electrode is fabricated in a circular shape.

9. An input/output protection device in accordance with one of claim 7 or 8, wherein the gate electrode is connected to the signal wiring of the internal circuit of the semiconductor integrated circuit.

10. An input/output protection device in accordance with one of claim 7 or 8, wherein the gate electrode is fixed to a predetermined potential.

11. An input/output protection device in accordance with one of claims 1 to 10, wherein:

the first conduction type is a p type and the second conduction type is an n type; and

the predetermined potential is a ground potential.

12. An input/output protection device in accordance with one of claims 1 to 10, wherein:

the first conduction type is an n type and the second conduction type is a p type; and

the predetermined potential is a potential of a power source.

ABSTRACT OF THE DISCLOSURE

An input/output protection device of lateral, bipolar type quickly responds to an excess voltage pulse and/or an excess current pulse of, for example, electrostatic discharge. In a region of a first conduction type (a fourth diffusion layer) of a semiconductor substrate, a first diffusion layer of a second conduction type opposite to the first conduction type is fabricated, the layer being connected to an input/output terminal. A second diffusion layer of the second conduction type is fabricated to be connected to electrode wiring at a fixed potential. A third diffusion layer of the second conduction type is manufactured at a bottom of the second diffusion layer and is connected to the second diffusion layer. The first diffusion layer is circularly enclosed with the third diffusion layer. When a high voltage is applied to the input/output terminal, a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

FIG. 1A

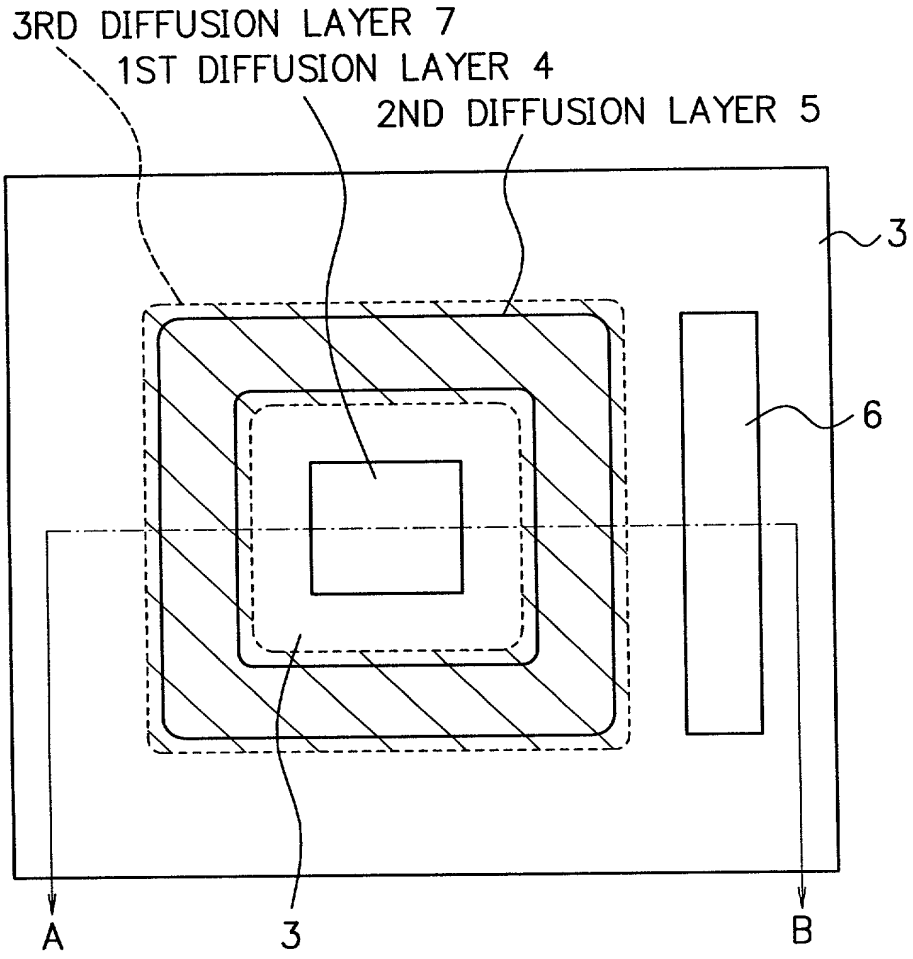

3RD DIFFUSION LAYER 7
1ST DIFFUSION LAYER 4
2ND DIFFUSION LAYER 5
3
6
A
3
B

FIG. 1B

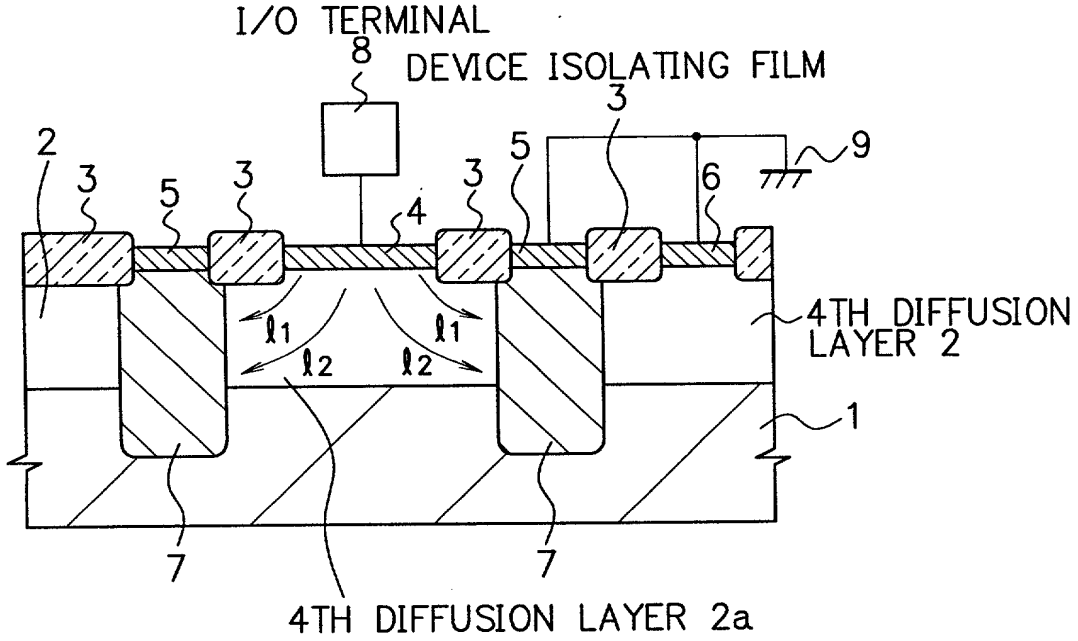
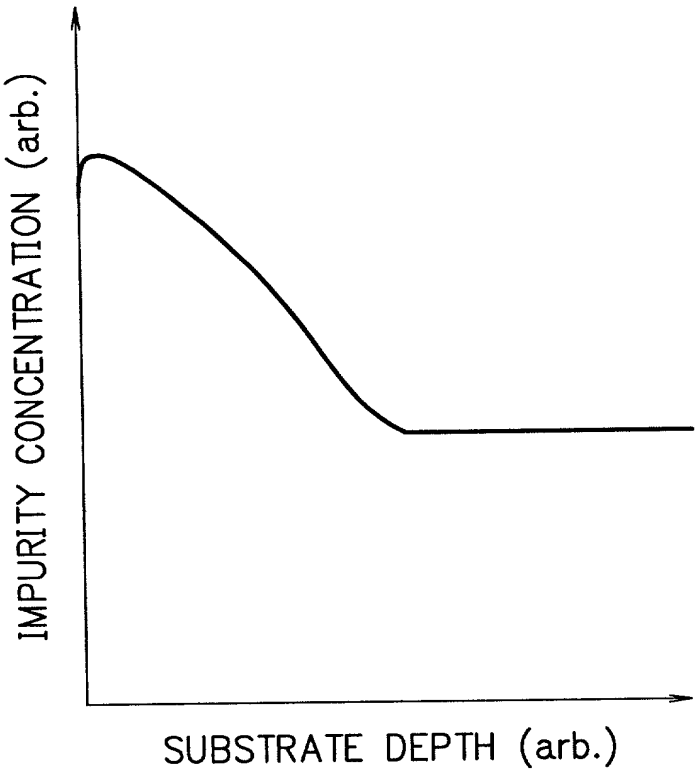
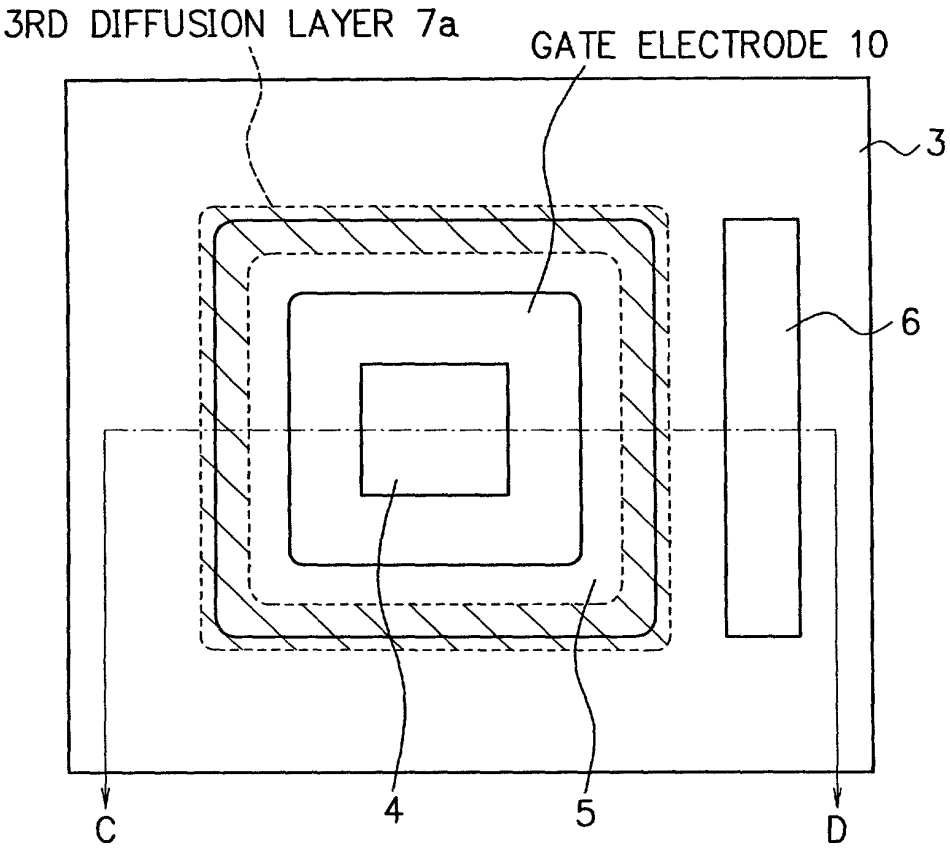

I/O TERMINAL
8
DEVICE ISOLATING FILM
3
2
3
5
3
3
5
9
6
4
4TH DIFFUSION LAYER 2
l1
l2
l1
l2
1
7
7
4TH DIFFUSION LAYER 2a

FIG. 2



F I G. 3A


3RD DIFFUSION LAYER 7a
GATE ELECTRODE 10
3
6
C
4
5
D

F I G. 3B

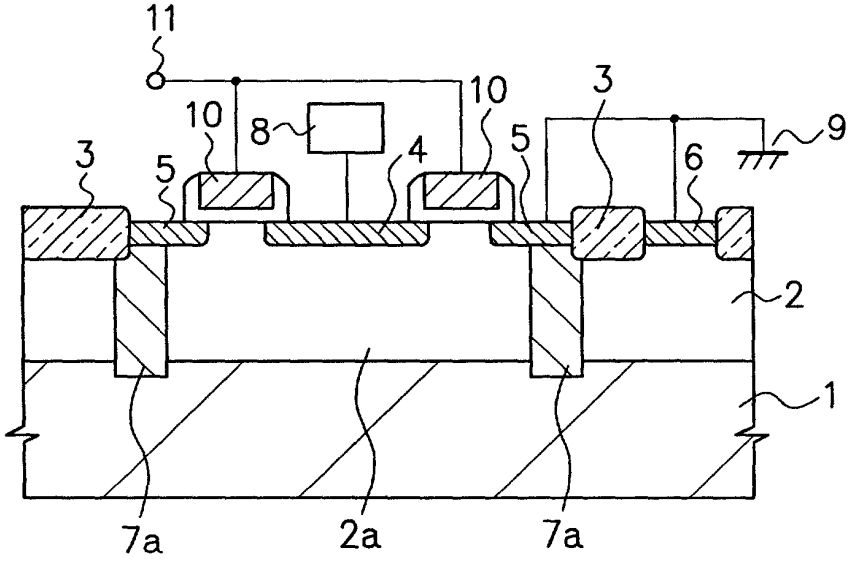

11
10
8
10
3
9
3
5
4
5
6
2
1
7a
2a
7a

FIG. 4

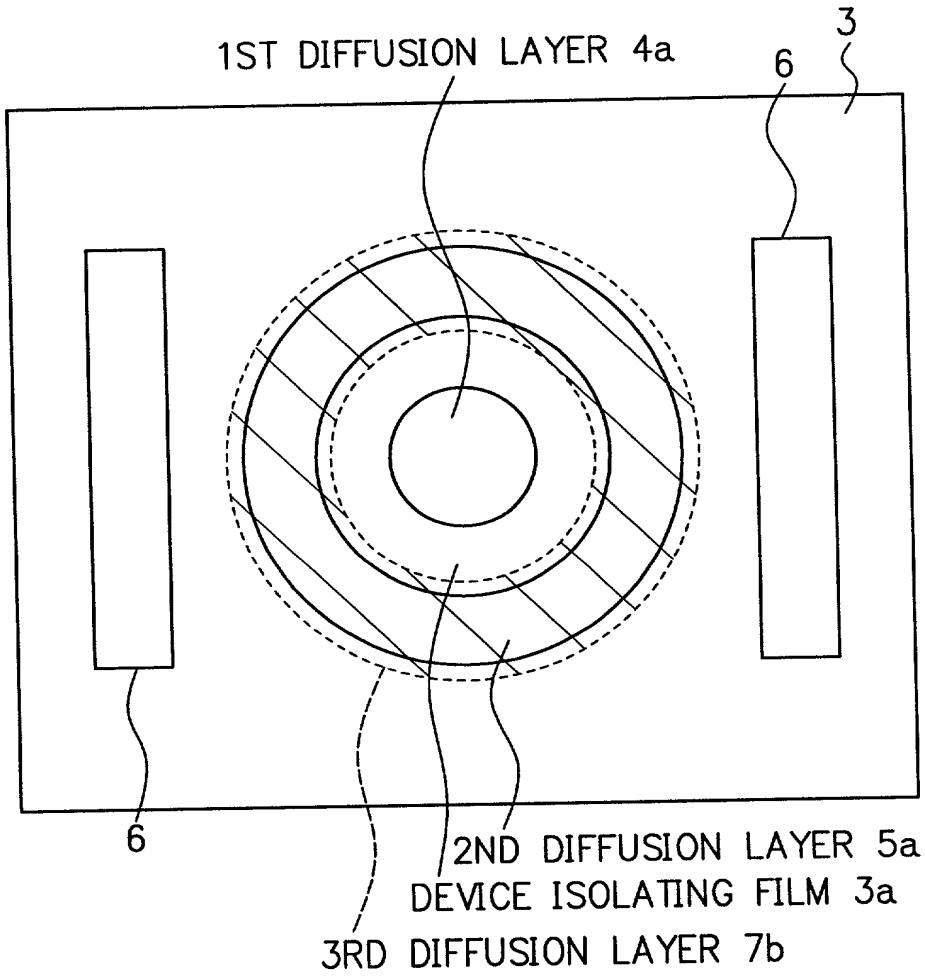

1ST DIFFUSION LAYER 4a
3
6
6
2ND DIFFUSION LAYER 5a
DEVICE ISOLATING FILM 3a
3RD DIFFUSION LAYER 7b

FIG. 5A

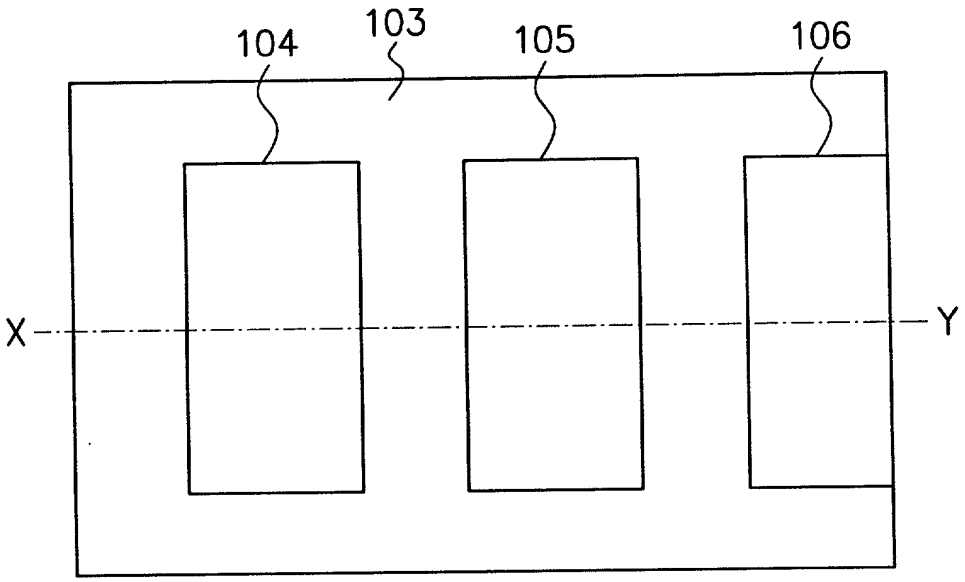
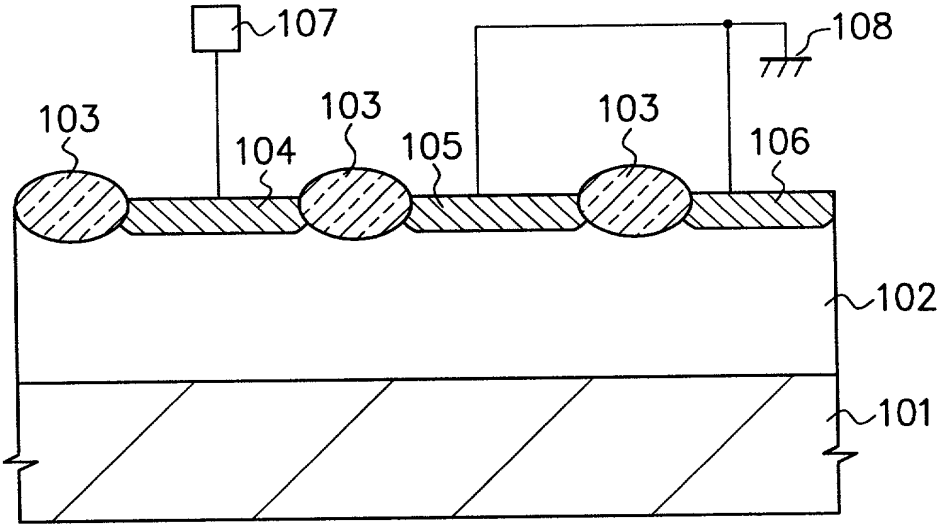


FIG. 5B



Application for United States Patent

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

AN INPUT/OUTPUT PROTECTION DEVICE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT

the specification of which:

(check one)

☒ is attached hereto

☐ was filed on _____, as
Application Serial No. _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56*

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			priority claimed	
204819/1999	Japan	19/7/1999	x	___
(Number)	(Country)	(Day/Month/Year Filed)	yes	no
___	___	___	___	___
(Number)	(Country)	(Day/Month/Year Filed)	yes	no
___	___	___	___	___
(Number)	(Country)	(Day/Month/Year Filed)	yes	no

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

Power of Attorney: As a named inventor, I hereby appoint Sean M. McGinn, Reg. 34,386, and Frederick W. Gibb, III, Reg. No. 37,629 as attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. All correspondence should be directed to McGinn & Gibb, P.C., 1701 Clarendon Boulevard, Suite 100, Arlington, Virginia 22201. Telephone calls should be directed to McGinn & Gibb, P.C. at (703) 294-6699.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the

United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____

Full Name of Third Joint Inventor, If Any _____

Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____

Full Name of Fourth Joint Inventor, If Any _____

Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____

(An additional sheet(s) is/are attached hereto if the present invention includes more than four inventors.)

*Title 37, Code of Federal Regulations, § 1.56:

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith toward the Patent and Trademark Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and (1) it establishes , by itself or in combination with other information, a prima facie case of unpatentability; or (2) it refutes, or is inconsistent with, a position the applicant takes in: (i) opposing an argument of unpatentability relied on by the Office, or (ii) asserting an argument of patentability.